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EXAMINER	
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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/066,651	KIM, JOO-SEON	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *23-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 28-30* is/are rejected.

7)☒ Claim(s) *17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4,5*.

4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *6* .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-22 and 28-30, drawn to A Reed-Solomon Decoder comprising: a Storing Part; a Calculation Part for Calculating an Error Location and an Error Value from (2m) Bit Data from the Storing Part; and a Control Part for Correcting an Error of the Data According to the Error Location and the Error Value; classified in class 714, subclass 784.

   II. Claims 23-27, drawn to An Error Correction Method for Inner and Outer Codes comprising Calculating a First Syndrome Polynomial from Inner Code Words Received in (2m) Bit Units; Calculating a Second Syndrome Polynomial from Inner Code Words Received in (2m) Bit Units; classified in class 714, subclass 756.

The inventions are distinct, each from the other because of the following reasons: Inventions Group I, A Reed-Solomon Decoder comprising: a Storing Part; a Calculation Part for Calculating an Error Location and an Error Value from (2m) Bit Data from the Storing Part; and a Control Part for Correcting an Error of the Data According to the Error Location and the Error Value; and Group II, An Error Correction Method for Inner and Outer Codes comprising Calculating a First Syndrome Polynomial from Inner Code Words Received in (2m) Bit Units; Calculating a Second Syndrome Polynomial from

Inner Code Words Received in (2m) Bit Units; are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I, A Reed-Solomon Decoder comprising: a Storing Part; a Calculation Part for Calculating an Error Location and an Error Value from (2m) Bit Data from the Storing Part; and a Control Part for Correcting an Error of the Data According to the Error Location and the Error Value; has separate utility such as for decoding parallel-concatenated Reed-Solomon Coded codewords. Group II, An Error Correction Method for Inner and Outer Codes comprising Calculating a First Syndrome Polynomial from Inner Code Words Received in (2m) Bit Units; Calculating a Second Syndrome Polynomial from Inner Code Words Received in (2m) Bit Units; has separate utility such as for decoding serial-concatenated Reed-Solomon Coded codewords. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Peter McKenna on 23 June 2004 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-22 and 28-30. Affirmation of this election must be made by applicant in replying to this Office action. Claims 23-27 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Oath/Declaration

The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

Applicant has not given a post office address anywhere in the application papers as required by 37 CFR 1.33(a), which was in effect at the time of filing of the oath or

declaration. A statement over applicant's signature providing a complete post office address is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-14, 28, 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. “m” in line 4 is undefined hence the value “2m” is undefined.

3. Claims 13, 14, 21, 22 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13 recites the limitation "the calculated eraser location polynomial" in line 6 and 7. There is insufficient antecedent basis for this limitation in the claim.

Claim 21 recites the limitation "the calculated eraser location polynomial" in line 6 and 7. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Massoudi; Firooz (US 6363511 B1).

35 U.S.C. 102(e) rejection of claim 1.

Massoudi teaches a Reed-Solomon decoder (Figure 6 in Massoudi is a Reed-Solomon decoder; see col. 7, lines 35-40 in Massoudi) comprising: a storing part (Figure 1A in Massoudi is a storing part); a calculation part for calculating an error location and an error value from 2m bit data from the storing part (Correction Engine 608 and Correction Circuit 602 in Figure 6 of Massoudi is a calculation part for calculating an error location and an error value from 2m bit data from the storing part; Note: Figure 2B in Massoudi teaches that column data has 192 bytes, i.e., 1536 bits, hence if m=768, a column has 2m data bits; See col. 9, lines 39-42 in Massoudi); and a control part for correcting an error of the data according to the error location and the error value, and controlling the calculation part to output a decoded signal (Correction Control Circuit in Figure 6 of Massoudi is a control part for correcting an error of the data according to the error location and the error value, and controlling the calculation part, Correction Engine 608 and Correction Circuit 602, to output a decoded signal to Correction Buffer 612; See col. 9, lines 31-67 and col. 10, lines 1-36 in Massoudi).

35 U.S.C. 102(e) rejection of claim 3.

Massoudi teaches a first RS core for calculating a first error location and a first error value from the data read from the storing part (On-The-Fly Row Correction Circuitry in Figure 6 of Massoudi is a first RS core for calculating a first error location and a first error value from the data read from the storing part); and a second RS core for calculating a second error location and a second error value from the data read from the storing part (Correction Circuitry 602 in Figure 6 of Massoudi is a second RS core for calculating a second error location and a second error value from the data read from the storing part).

35 U.S.C. 102(e) rejection of claim 10.

Massoudi teaches a Reed-Solomon decoder for processing (m) or (2m) bit data (Figure 6 in Massoudi is a Reed-Solomon decoder; see col. 7, lines 35-40 in Massoudi; Note: Figure 2B in Massoudi teaches that column data has 192 bytes, i.e., 1536 bits, hence if m=768, a column has 2m data bits; See col. 9, lines 39-42 in Massoudi), comprising: a storing part for storing (2m) bit data (Figure 1A in Massoudi is a storing part); a main control part for controlling the storing part (Disc Controller 402 in Figure 4A of Massoudi is a main control part for controlling the storing part); a first RS core for calculating a first error location and a first error value from the data read from the storing part (On-The-Fly Row Correction Circuitry in Figure 6 of Massoudi is a first RS core for calculating a first error location and a first error value from the data read from the storing part); a first RS

core control part for controlling the first RS core under the control of the main control part (Correction Control Circuit in Figure 6 of Massoudi is a first RS core control part for controlling the first RS core under the control of the main control part); a second RS core for calculating a second error location and a second error value from the data read from the storing part (On-The-Fly Row Correction Manger 804 in Correction Circuitry 602 in Figures 6 & 8 of Massoudi is a second RS core for calculating a second error location and a second error value from the data read from the storing part); and a second RS core control part for controlling the second RS core under the control of the main control part (Repeat Correction Manager 812 in Correction Control Circuit in Figures 6 & 8 of Massoudi is second RS core control part for controlling the second RS core under the control of the main control part).

5. Claims 15 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujita; Hachiro et al. (US 6131178 A, hereafter referred to as Fujita).

35 U.S.C. 102(e) rejection of claim 15.

Fujita teaches a Reed-Solomon decoding method comprising the steps of: reading data to be decoded and an eraser flag (Figure 21 in Fujita teaches that erasure flags are read from storage and Figure 24 in Fujita teaches an erasure locator generating step for generating an eraser location polynomial from an eraser flag read from the storing part); calculating an error location and an error value from the read data (the Berlekamp-Massey Algorithm in Step ST32 in Figure 24 of Fujita is a step for calculating a first

errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial); and correcting an error of the data according to the calculated error location and error value, and decoding the data (Step ST35 in Figure 24 of Fujita is a step for correcting an error of the data according to the calculated error location and error value, and decoding the data).

35 U.S.C. 102(e) rejection of claim 16.

Figure 6 in Massoudi is a Reed-Solomon decoder; see col. 7, lines 35-40 in Massoudi; Note: Figure 2B in Massoudi teaches that column data has 192 bytes, i.e., 1536 bits, hence if m=768, a column has 2m data bits; See col. 9, lines 39-42 in Massoudi.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 4-9, 11-14, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Massoudi; Firooz (US 6363511 B1) in view of Fujita; Hachiro et al. (US 6131178 A, hereafter referred to as Fujita).

35 U.S.C. 103(a) rejection of claims 4 and 11.

Massoudi substantially teaches the claimed invention described in claims 1, 3 and 10 (as rejected above). In addition, Massoudi teaches a first syndrome polynomial calculation part for calculating a first syndrome polynomial from the data read from the storing part (Row Syndrome Generator Circuitry 604 in Figure 6 of Massoudi is a first syndrome polynomial calculation part for calculating a first syndrome polynomial from the data read from the storing part); a first errata location polynomial calculation part (On-The-Fly Row Correction Circuitry in Figure 6 of Massoudi is a first errata location polynomial calculation part; Note: error location polynomials are inherently used in a Reed-Solomon Error Correction device), and outputting the first errata location polynomial and the delayed first syndrome polynomial (Row Syndrome Generator Circuitry 604 and On-The-Fly Row Correction Circuitry 410 in Figure 6 of Massoudi output the first errata location polynomial and the delayed first syndrome polynomial); and a first error location/value calculation part for calculating a first error flag, a first error location and a first error value from the first errata location polynomial and the delayed first syndrome polynomial (col. 6, lines 52-54 in Massoudi teach that the Row Syndrome Generator Circuitry 604 and On-The-Fly Row Correction Circuitry 410 in Figure 6 of Massoudi generates row erasure pointers, a first error location and a first

error value from the first errata location polynomial and the delayed first syndrome polynomial; Note: a row erasure pointer is a first error flag).

However Massoudi does not explicitly teach the specific use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part; and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial.

Fujita, in an analogous art, teaches use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part (Figure 21 in Fujita teaches that erasure flags are read from storage and Figure 24 in Fujita teaches an erasure locator generating step for generating an eraser location polynomial from an eraser flag read from the storing part); and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial (the Berlekamp-Massey Algorithm in Step ST32 in Figure 24 of Fujita is a step for calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial). Note: Massoudi teaches a Reed-Solomon error correction device, but does not teach the details of the Reed-Solomon error correction device; Fujita , on the other hand, teaches the required details of a Reed-Solomon error correction device required to implement the Reed-Solomon error correction device taught in the Massoudi patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Massoudi with the teachings of Fujita by including use of an eraser location polynomial calculation part for calculating an eraser location

polynomial from an eraser flag read from the storing part; and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part; and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial would have provided the opportunity to implement the Reed-Solomon error correction device taught in the Massoudi patent.

35 U.S.C. 103(a) rejection of claim 5.

The syndrome equations in claim 5 are obvious mathematically derivations of syndrome equations for a particular embodiment of the teachings in the Massoudi and Fujita patents.

35 U.S.C. 103(a) rejection of claims 6 and 12.

Massoudi and Fujita substantially teaches the claimed invention described in claims 1, 3 and 4 (as rejected above).

However Massoudi and Fujita do not explicitly teach the specific use of a specific hardware embodiment for implementing the circuitry of the Applicant's claim 6.

The Examiner asserts that one of ordinary skill in the art at the time the invention was made would have known how to and would have been highly motivated to create a

specific hardware embodiment for implementing the circuitry of the Applicant's claim 6 based on obvious engineering design choices in order to implement the design in the Massoudi patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Massoudi and Fujita by including use of a specific hardware embodiment for implementing the circuitry of the Applicant's claim 6. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a specific hardware embodiment for implementing the circuitry of the Applicant's claim 6 would have provided the opportunity to implement the design in the Massoudi patent.

35 U.S.C. 103(a) rejection of claim 7.

Massoudi teaches a second syndrome polynomial calculation part for calculating a second syndrome polynomial from the data read from the storing part (Column and EDC Syndrome Generator Circuitry 412 in Figure 6 of Massoudi is a second syndrome polynomial calculation part for calculating a second syndrome polynomial from the data read from the storing part); a second errata location polynomial calculation part for calculating a second errata location polynomial from the calculated eraser location polynomial and second syndrome polynomial (Correction Circuitry 602 in Figure 6 is a second errata location polynomial calculation part for calculating a second errata location polynomial from the calculated eraser location polynomial and second

syndrome polynomial), and outputting the second errata location polynomial and the delayed second syndrome polynomial (Column and EDC Syndrome Generator Circuitry 412 and Correction Circuitry 602 in Figure 6 of Massoudi output the second errata location polynomial and the delayed second syndrome polynomial); and a second error location/value calculation part for calculating a second error flag, a second error location and a second error value from the second errata location polynomial and the delayed second syndrome polynomial (col. 10, lines 6-18 in Massoudi teach that the second error location/value calculation part, Column and EDC Syndrome Generator Circuitry 412 and Correction Circuitry 602 in Figure 6 of Massoudi, calculates a second error flag, a second error location and a second error value from the second errata location polynomial and the delayed second syndrome polynomial).

35 U.S.C. 103(a) rejection of claim 8.

The syndrome equations in claim 8 are obvious mathematically derivations of syndrome equations for a particular embodiment of the teachings in the Massoudi and Fujita patents.

35 U.S.C. 103(a) rejection of claim 9.

Massoudi and Fujita substantially teaches the claimed invention described in claims 1 and 3-8 (as rejected above).

However Massoudi and Fujita do not explicitly teach the specific use of a specific hardware embodiment for implementing the circuitry of the Applicant's claim 9.

The Examiner asserts that one of ordinary skill in the art at the time the invention was made would have known how to and would have been highly motivated to create a specific hardware embodiment for implementing the circuitry of the Applicant's claim 9 based on obvious engineering design choices in order to implement the design in the Massoudi patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Massoudi and Fujita by including use of a specific hardware embodiment for implementing the circuitry of the Applicant's claim 9. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a specific hardware embodiment for implementing the circuitry of the Applicant's claim 6 would have provided the opportunity to implement the design in the Massoudi patent.

35 U.S.C. 103(a) rejection of claim 13.

Massoudi substantially teaches the claimed invention described in claims 1 and 3-12 (as rejected above). In addition, Massoudi teaches a second syndrome polynomial calculation part for calculating a first syndrome polynomial from the data read from the storing part (Column and EDC Syndrome Generator Circuitry 412 in Figure 6 of Massoudi is a second syndrome polynomial calculation part for calculating a second syndrome polynomial from the data read from the storing part); a second errata location polynomial calculation part (Correction Circuitry 602 in Figure 6 of Massoudi is a second

errata location polynomial calculation part; Note: error location polynomials are inherently used in a Reed-Solomon Error Correction device), and outputting the second errata location polynomial and the delayed second syndrome polynomial (Column and EDC Syndrome Generator Circuitry 412 and Correction Circuitry 602 in Figure 6 of Massoudi output the second errata location polynomial and the delayed second syndrome polynomial); and a second error location/value calculation part for calculating a second error flag, a first error location and a second error value from the second errata location polynomial and the delayed first syndrome polynomial (col. 10, lines 6-18 in Massoudi teach that the second error location/value calculation part, Column and EDC Syndrome Generator Circuitry 412 and Correction Circuitry 602 in Figure 6 of Massoudi, calculates a second error flag, a second error location and a second error value from the second errata location polynomial and the delayed second syndrome polynomial).

However Massoudi does not explicitly teach the specific use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part; and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial.

Fujita, in an analogous art, teaches use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part (Figure 21 in Fujita teaches that erasure flags are read from storage and Figure 24 in Fujita teaches an erasure locator generating step for generating an eraser location polynomial from an eraser flag read from the storing part); and calculating a first errata

location polynomial from the calculated eraser location polynomial and first syndrome polynomial (the Berlekamp-Massey Algorithm in Step ST32 is a step for calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial). Note: Massoudi teaches a Reed-Solomon error correction device, but does not teach the details of the Reed-Solomon error correction device; Fujita , on the other hand, teaches the required details of a Reed-Solomon error correction device required to implement the Reed-Solomon error correction device taught in the Massoudi patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Massoudi with the teachings of Fujita by including use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part; and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part; and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial would have provided the opportunity to implement the Reed-Solomon error correction device taught in the Massoudi patent.

35 U.S.C. 103(a) rejection of claim 14.

Massoudi and Fujita substantially teaches the claimed invention described in claims 1 and 3-13 (as rejected above).

However Massoudi and Fujita do not explicitly teach the specific use of a specific hardware embodiment for implementing the circuitry of the Applicant's claim 13.

The Examiner asserts that one of ordinary skill in the art at the time the invention was made would have known how to and would have been highly motivated to create a specific hardware embodiment for implementing the circuitry of the Applicant's claim 13 based on obvious engineering design choices in order to implement the design in the Massoudi patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Massoudi and Fujita by including use of a specific hardware embodiment for implementing the circuitry of the Applicant's claim 13. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a specific hardware embodiment for implementing the circuitry of the Applicant's claim 13 would have provided the opportunity to implement the design in the Massoudi patent.

35 U.S.C. 103(a) rejection of claims 28 and 29.

The syndrome equations in claims 28 and 29 are obvious mathematically derivations of syndrome equations for a particular embodiment of the teachings in the Massoudi and Fujita patents.

7. Claims 18-22 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujita; Hachiro et al. (US 6131178 A, hereafter referred to as Fujita) in view of Massoudi; Firooz (US 6363511 B1).

35 U.S.C. 103(a) rejection of claim 18.

Fujita substantially teaches the claimed invention described in claim 18 (as rejected above).

However Fujita does not explicitly teach the specific use of two Reed-Solomon Encoders for a product code.

Massoudi, in an analogous art, teaches use of two Reed-Solomon Encoders for a product code (see Figure 6 in Massoudi). In particular, Massoudi teaches a first RS core for calculating a first error location and a first error value from the data read from the storing part (On-The-Fly Row Correction Circuitry in Figure 6 of Massoudi is a first RS core for calculating a first error location and a first error value from the data read from the storing part); and a second RS core for calculating a second error location and a second error value from the data read from the storing part (Correction Circuitry 602 in Figure 6 of Massoudi is a second RS core for calculating a second error location and a second error value from the data read from the storing part).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Fujita with the teachings of Massoudi by including use of two Reed-Solomon Encoders for a product code. This modification would have been

obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of two Reed-Solomon Encoders for a product code would have provided the opportunity to decode a serially-concatenated Reed-Solomon code.

35 U.S.C. 103(a) rejection of claim 19.

Massoudi teaches a first syndrome polynomial calculation part for calculating a first syndrome polynomial from the data read from the storing part (Row Syndrome Generator Circuitry 604 in Figure 6 of Massoudi is a first syndrome polynomial calculation part for calculating a first syndrome polynomial from the data read from the storing part); a first errata location polynomial calculation part (On-The-Fly Row Correction Circuitry in Figure 6 of Massoudi is a first errata location polynomial calculation part; Note: error location polynomials are inherently used in a Reed-Solomon Error Correction device), and outputting the first errata location polynomial and the delayed first syndrome polynomial (Row Syndrome Generator Circuitry 604 and On-The-Fly Row Correction Circuitry 410 in Figure 6 of Massoudi output the first errata location polynomial and the delayed first syndrome polynomial); and a first error location/value calculation part for calculating a first error flag, a first error location and a first error value from the first errata location polynomial and the delayed first syndrome polynomial (col. 6, lines 52-54 in Massoudi teach that the Row Syndrome Generator Circuitry 604 and On-The-Fly Row Correction Circuitry 410 in Figure 6 of Massoudi generates row erasure pointers, a first error location and a first error value from the first

errata location polynomial and the delayed first syndrome polynomial; Note: a row erasure pointer is a first error flag).

Fujita, in an analogous art, teaches use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part (Figure 21 in Fujita teaches that erasure flags are read from storage and Figure 24 in Fujita teaches an erasure locator generating step for generating an eraser location polynomial from an eraser flag read from the storing part); and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial (the Berlekamp-Massey Algorithm in Step ST32 in Figure 24 of Fujita is a step for calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial). Note: Massoudi teaches a Reed-Solomon error correction device, but does not teach the details of the Reed-Solomon error correction device; Fujita , on the other hand, teaches the required details of a Reed-Solomon error correction device required to implement the Reed-Solomon error correction device taught in the Massoudi patent.

35 U.S.C. 103(a) rejection of claim 20.

The syndrome equations in claim 20 are obvious mathematically derivations of syndrome equations for a particular embodiment of the teachings in the Massoudi and Fujita patents.

35 U.S.C. 103(a) rejection of claim 21.

Massoudi teaches a second syndrome polynomial calculation part for calculating a first syndrome polynomial from the data read from the storing part (Column and EDC Syndrome Generator Circuitry 412 in Figure 6 of Massoudi is a second syndrome polynomial calculation part for calculating a second syndrome polynomial from the data read from the storing part); a second errata location polynomial calculation part (Correction Circuitry 602 in Figure 6 of Massoudi is a second errata location polynomial calculation part; Note: error location polynomials are inherently used in a Reed-Solomon Error Correction device), and outputting the second errata location polynomial and the delayed second syndrome polynomial (Column and EDC Syndrome Generator Circuitry 412 and Correction Circuitry 602 in Figure 6 of Massoudi output the second errata location polynomial and the delayed second syndrome polynomial); and a second error location/value calculation part for calculating a second error flag, a first error location and a second error value from the second errata location polynomial and the delayed first syndrome polynomial (col. 10, lines 6-18 in Massoudi teach that the second error location/value calculation part, Column and EDC Syndrome Generator Circuitry 412 and Correction Circuitry 602 in Figure 6 of Massoudi, calculates a second error flag, a second error location and a second error value from the second errata location polynomial and the delayed second syndrome polynomial).

Fujita, in an analogous art, teaches use of an eraser location polynomial calculation part for calculating an eraser location polynomial from an eraser flag read from the storing part (Figure 21 in Fujita teaches that erasure flags are read from storage and Figure 24 in Fujita teaches an erasure locator generating step for generating an eraser location

polynomial from an eraser flag read from the storing part); and calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial (the Berlekamp-Massey Algorithm in Step ST32 is a step for calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial). Note: Massoudi teaches a Reed-Solomon error correction device, but does not teach the details of the Reed-Solomon error correction device; Fujita , on the other hand, teaches the required details of a Reed-Solomon error correction device required to implement the Reed-Solomon error correction device taught in the Massoudi patent.

35 U.S.C. 103(a) rejection of claim 22.

The syndrome equations in claim 22 are obvious mathematically derivations of syndrome equations for a particular embodiment of the teachings in the Massoudi and Fujita patents.

35 U.S.C. 103(a) rejection of claim 30.

Massoudi teaches a first RS core for calculating a first error location and a first error value from the data read from the storing part (On-The-Fly Row Correction Circuitry in Figure 6 of Massoudi is a first RS core for calculating a first error location and a first error value from the data read from the storing part); and a second RS core for calculating a second error location and a second error value from the data read from the storing part (Correction Circuitry 602 in Figure 6 of Massoudi is a second RS core for

calculating a second error location and a second error value from the data read from the storing part).

Allowable Subject Matter

8. Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The present invention pertains to a method for a Reed-Solomon decoding method comprising the steps of: reading data to be decoded and an eraser flag; calculating an error location and an error value from the read data; and correcting an error of the data according to the calculated error location and error value, and decoding the data.

Claim 17 recites various features:

"an eraser location polynomial calculation step for calculating an eraser location polynomial from the read eraser flag; a first syndrome polynomial calculation step for calculating a first syndrome polynomial from the read data; a second syndrome polynomial calculation step for calculating a second syndrome polynomial from the read data; a first errata location polynomial calculation step for calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial, and outputting the first errata location polynomial and the delayed first

syndrome polynomial; a first error location/value calculation step for calculating a first error flag, a first error location and a first error value from the first errata location polynomial and the delayed first syndrome polynomial; a second errata location polynomial calculation step for calculating a second errata location polynomial from the calculated eraser location polynomial and second syndrome polynomial, and outputting the second errata location polynomial and the delayed second syndrome polynomial; and a second error location/value calculation step for calculating a second error flag, a second error location and a second error value from the second errata location polynomial and the delayed second syndrome polynomial".

Fujita (US 6131178 A) teaches a Reed-Solomon decoding method comprising the steps of: reading data to be decoded and an eraser flag (Figure 21 in Fujita teaches that erasure flags are read from storage and Figure 24 in Fujita teaches an erasure locator generating step for generating an eraser location polynomial from an eraser flag read from the storing part); calculating an error location and an error value from the read data (the Berlekamp-Massey Algorithm in Step ST32 in Figure 24 of Fujita is a step for calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial); and correcting an error of the data according to the calculated error location and error value, and decoding the data (Step ST35 in Figure 24 of Fujita is a step for correcting an error of the data according to the calculated error location and error value, and decoding the data).

The prior art however are not concerned with and do not teach, suggest, or otherwise render obvious the algorithm for an eraser location polynomial calculation step for

calculating an eraser location polynomial from the read eraser flag; a first syndrome polynomial calculation step for calculating a first syndrome polynomial from the read data; a second syndrome polynomial calculation step for calculating a second syndrome polynomial from the read data; a first errata location polynomial calculation step for calculating a first errata location polynomial from the calculated eraser location polynomial and first syndrome polynomial, and outputting the first errata location polynomial and the delayed first syndrome polynomial; a first error location/value calculation step for calculating a first error flag, a first error location and a first error value from the first errata location polynomial and the delayed first syndrome polynomial; a second errata location polynomial calculation step for calculating a second errata location polynomial from the calculated eraser location polynomial and second syndrome polynomial, and outputting the second errata location polynomial and the delayed second syndrome polynomial; and a second error location/value calculation step for calculating a second error flag, a second error location and a second error value from the second errata location polynomial and the delayed second syndrome polynomial as taught by claim 17 and its base and intervening claims. Hence the prior art taken alone or in any combination fail to teach the claimed novel feature in claim 17 in view of its base and intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chapman; Ronald James et al. (US 6367046 B1) teaches error detection and correction Systems for digital data communication, processing storage and retrieval systems. Sako; Yoichiro et al. (US 4881232 A) teaches a method and apparatus suitable for faithfully and accurately reproducing data from each sector of a track on a disk-shaped recording medium, such as a magneto-optic disk. Shikakura; Akihiro (US 5996109 A) teaches a circuit for detecting and correcting an error of a code train transmitted via a transmission path such as a magnetic recording/reproducing system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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